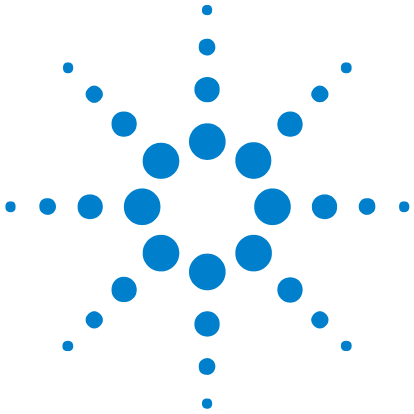

Agilent B4622A DDR Protocol Compliance and Analysis Tool

Help

Agilent Technologies

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DDR Validation—At a Glance

The DDR validation tool evaluates captured DDR2/DDR3 data against a set of user-defined limits to help you validate that a memory system is operating properly. The automated test application guides you through the process of selecting and configuring tests, running tests, and evaluating the test results.

The application assumes that the Agilent logic analysis system has already been set up to properly capture DDR data.

To use the automated test application, see:

Contents

1 About the Validation Tool

Overview of the tests

There are two types of tests:

- Tests which check for timing violations
- Tests which check for illegal DDR state transitions

The test limits can be (and must be) configured by the user.

The provided timing violation tests include:

Table 1 Timing violation tests

Parameter	Description	Test
$tRAS_{max}$	Row Active time ACTIVATE to PRECHARGE/Auto-PRECHARGE	must be < tRASmax
$tRAS_{min}$	Row Active time ACTIVATE to PRECHARGE/Auto-PRECHARGE	must be > tRASmin
tRP	PRECHARGE to any other command (same bank)	must be > tRP
tCCD	Time between any read or write command	must be > tCCD
tRRD	ACTIVATE to ACTIVATE (any bank)	must be >= tRRD
tFAW	Time for four ACTIVATEs (any bank)	must be >= tFAW
tRFC	REFRESH to REFRESH or ACTIVATE	must be > tRFC
tDARW	ACTIVATE to external READ/WRITE	must be > tDARW
tDRP	Read to Precharge/AutoPrecharge	must be > tDRP
tDRW	Read to Write	must be > tDRW
tDWP	Write to Precharge/AutoPrecharge	must be > tDWP
tDWR	Write to Read	must be > tDWR

Table 2 State machine violation tests

Description
READ or WRITE to an inactive row

Table 2 State machine violation tests (continued)

Description
REFRESH to an active bank
ACTIVATE to an active bank

Compatibility

The DDR validation tool works for most DDR2 and DDR3 systems.

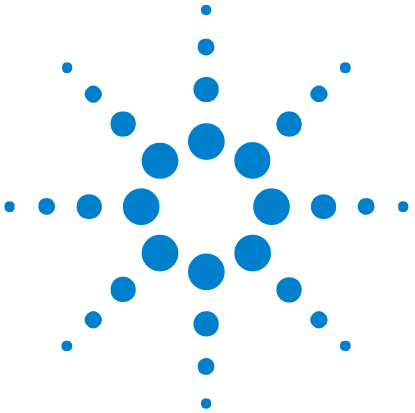
The validation tool is not able to fully model systems which use the following optional DDR features:

- Partial Array Self-Refresh (PASR)
- Auto Self-Refresh (ASR)
- On-the-fly Burst Length switching

About the software

The DDR validation tool is part of the Agilent B4622A Protocol Compliance and Analysis package.

The application uses the same software framework which is used by Agilent Infiniium oscilloscopes.



2 What's New

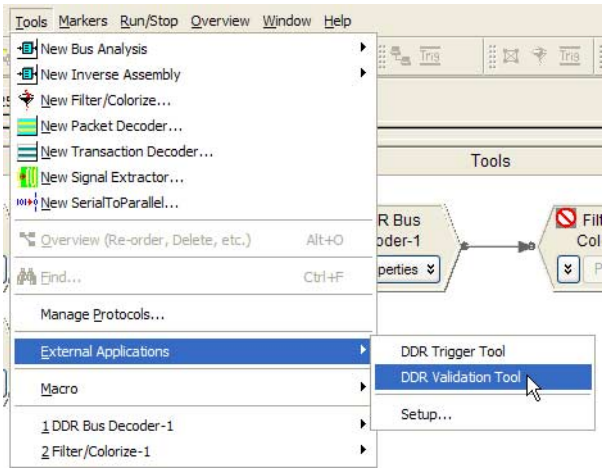
The following changes may be significant if you have created customized tests with a previous version of the to the DDR validation tool. This is not an exhaustive list of all changes.

Version 3.82 (Initial Release)

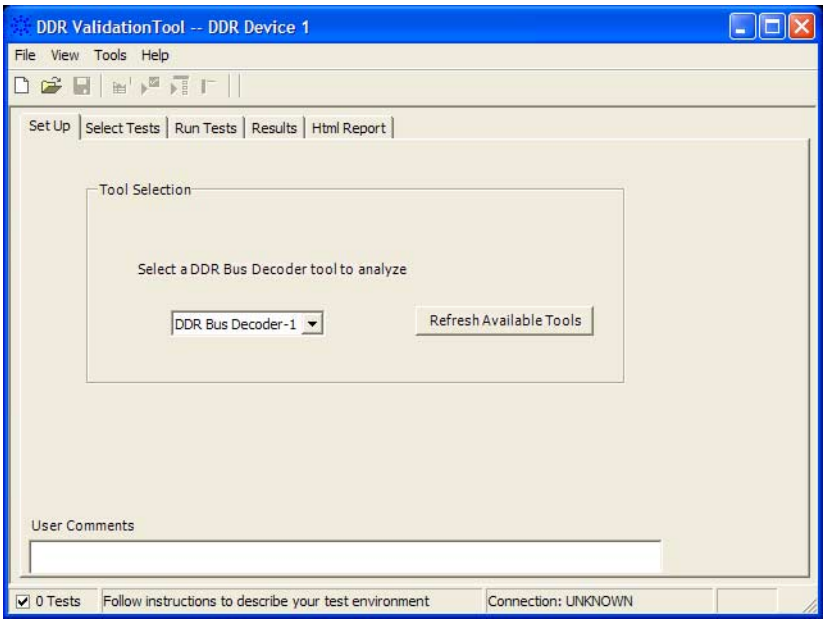
- Initial release.
- Requires version 3.80 or greater of the logic analysis system software.
- Requires version 3.81.4041 or greater of the Agilent B4621A bus decoder for DDR2 and DDR3.

3 Starting the DDR Validation Tool

1 From the logic analysis system's main menu, choose **Tools>External Applications>DDR Validation Tool**.



The DDR validation tool window appears.



See Also • "To view/hide the toolbar" on page 13

Next

- "Creating or Opening a Test Project" on page 45

To view/hide the toolbar

- To toggle between a hidden and visible toolbar, choose **View>Toolbar** from the menu.

4 Configuring Tests

You must configure a set of limits before you can run any tests.

These limits describe the memory part you are using and certain characteristics of the memory bus.

You can load, edit, and save limits from the **Tools>Compliance limits** menu.

See Also

- "To set the test limits" on page 16 (for information on how to calculate the limits)
- "To create/edit limit sets" on page 21 (for information on how to enter and save the limits)
- "To activate/refresh limit sets" on page 25 (for information on how to load a limit set which you have saved)

To set the test limits

All timing violation tests are based on compliance limits that are specified by the user. Specify these limits based on the specific DDR memory parts you are using. Limits will vary depending on:

- Memory technology (DDR2, DDR3)
- Speed grade
- Clock speed
- Part density
- User selected options such as Additive Latency and burst length

Units

Some times must be entered in seconds (s). If the data sheet expresses these limits in terms of clock cycles, you will need to convert those limits to seconds.

Each logic analyzer sample has a timestamp. Results will be calculated by subtracting the time stamp of the first event from the timestamp of the second event. Note that the time stamps are only as good as the time stamp resolution of the logic analyzer card being used (this resolution may be as coarse as 2ns; see the Specifications and Characteristics in the logic analyzer's online help for details). The elapsed time includes time during which the DDR clock is inactive.

Other times must be entered as a number of clock cycles (CK). Results will be calculated by counting the number of logic analyzer samples between the two events.

Additive latency (AL) is normally expressed as a number of clocks (CK). For some calculations, you will need to convert AL to seconds (s) by dividing by the clock rate.

Burst length (BL) is simply an integer (4 or 8).

Definitions of the limits

You will need to look up some of the limits from the part data sheet. You will then calculate values for the derived limits.

Agilent suggests using the formulas here to compute the derived limits. However, it is entirely the responsibility of the user to choose limits that are appropriate for the intended application.

Here are the limits you need to specify:

Table 3 Limits used by the tests

Parameter	Description	Unit	Suggested Definition	Reference
$tRAS_{max}$	Row Active time ACTIVE to PRECHARGE	s	Part dependent (9 * tREFI)	Data Sheet (tREFI). See DDR3 (see) page 147.
$tRAS_{min}$	Row Active time ACTIVE to PRECHARGE	s	Part dependent	Data Sheet
tDARW	Min ACT to external READ/WRITE	s	tRCD-AL	DDR2 (see) 3.5 / DDR3 (see) 12.3
tRP	Row Precharge time min PRECHARGE to any other command (same bank)	s	Part dependent	Data Sheet
tDRP	Min Read to Precharge	CK	DDR2: AL + BL/2 + max (tRTP, 2CK) -2CK DDR3: AL + tRTP	DDR2 (see) 3.7.1 / DDR3 (see) 4.13.3
tDRW	Min Read to Write	CK	DDR2: BL/2 + 2CK DDR3: BL4: RL + CCD/2 + 2CK – WL DDR3: BL8: RL + CCD + 2CK - WL	DDR2 (see) figure 35 / DDR3 (see) figure 35, 36
tRFC	REFRESH command time. min time REFRESH to REFRESH or ACTIVATE	s	Part dependent	Data Sheet
tDWP	Min Write to Precharge	CK	WL + BL/2 + tWR	DDR2 (see) 3.7.2 / DDR3 (see) Figure 49, 50
tDWR	Min Write to Read	CK	DDR2: CL -1 + BL/2 + tWTR DDR3: WL + BL/2 + tWTR	DDR2 (see) Figure 41 / DDR3 (see) Figure 53, 56
tCCD	CAS to CAS delay min time between any read or write command	CK	Part dependent	Data Sheet
tRRD	Min time between two ACTIVATE commans (different banks)	s	Part dependent	Data Sheet
tFAW	Min time for four ACTIVATE commands (different banks)	s	Part dependent	Data Sheet

Values used to calculate the limits

To calculate the limits, you will need to look up or calculate the following values:

Table 4 Values used to calculate the limits

Parameter	Description	Unit	Suggested Definition	Reference
AL	Additive Latency	CK, s	User selection	System Design
BL	Burst Length		User selection	System Design
CL	CAS (Read) Latency	CK	Part dependent	Data Sheet
CWL	CAS Write Latency	CK	Part dependent	Data Sheet
RL	Read Latency	CK	AL + CL	DDR3 (see) 3.4.3.4
WL	Write latency	CK	AL + CWL	DDR3 (see) 3.4.3.4
tRCD	RAS to CAS Delay (ACT to internal R/W)	s	Part dependent	Data Sheet
tREFI	Refresh Interval; average time between Refresh commands	s	Part dependent	Data Sheet
tRTP	Internal Read to Precharge	s	Part dependent (max 4CK or 7.5ns)	Data Sheet
tWR	Internal Write Recovery	s	Part dependent	Data Sheet
tWTR	Internal Write to internal Read	s	Part dependent (max 4CK or 7.5ns)	Data Sheet

External Read/Write + AL = Internal Read/Write

Naming conventions

Limits which are normally expressed as maximum or minimum times have names beginning with 't'.

The names of derived timing limits begin with 'tD'. Derived limits are not usually specified directly in the part data sheet. In general, you will compute these from the standard timing parameters.

Limits which are normally expressed as a number of clock cycles have no prefix. In some cases, you may need to convert these to seconds for use by the tool.

Customizing the limits

The definitions are suggestions based on the DDR2/3 standards. There is no requirement that the user must set the limits to those specified in the data sheet or in the JEDEC standard. You can set the limits however you like, depending on the goals of your testing.

Example limits

An example limit set is supplied with the validation tool. The example is based on a DDR800 part with 6-6-6 timing.

To load and view the example limits, select **Tools>Compliance Limits>Create/Edit Limit Set**, then select **Load Limit Set...**, select **Official limit sets**, then select **DDR Example**.

Example part:

- Data sheet: MICRON DDR3 MT41J256-32 Me x 4 x 8 Banks PDF: 09005aef82f1e6e2 Rev. M 9/08 EN
- Speed Grade 25 (6-6-6)
- Clock 400 MHz (2.5ns)
- Data Rate 800 MT/s
- Temperature 0-85C

Table 5 Standard parameters used for example limit set

Parameter	Value	Reference
tREFI	7.8 us (low temp)	Data Sheet, page 71
$tRAS_{max}$	70.2us	Data Sheet (tREFI), page 63
$tRAS_{min}$	37.5ns	Data Sheet, page 30
tRP	15ns	Data Sheet, page 30
tCCD	4CK (10ns)	Data Sheet, page 70
tRRD	10ns	Data Sheet, page 30
tFAW	50ns	Data Sheet, page 30
tRFC	110ns	Data Sheet, page 30
tRCD	15ns	Data Sheet, page 30
tRTP	10ns	Data Sheet, page 70
tWR	15ns	Data Sheet, page 70
tWTR	10ns	Data Sheet, page 70
AL	0ns (0CK)	User selected (MR1, 0 means no additive latency)
BL	10ns (8 bursts)	User selected (MR0)
CL	6CK (15ns)	Data Sheet, page 30 (MR0)
CWL	5CK (12.5ns)	Data Sheet, page 116 (MR2)

Table 6 Derived values used for example limit set

Parameter	Value
RL	6CK (15ns)
WL	5CK (12.5ns)
tDARW	15ns
tDRP	10ns

Table 6 Derived values used for example limit set (continued)

Parameter	Value
tDRW	17.5ns
tDWP	32.5ns
tDWR	27.5ns

References

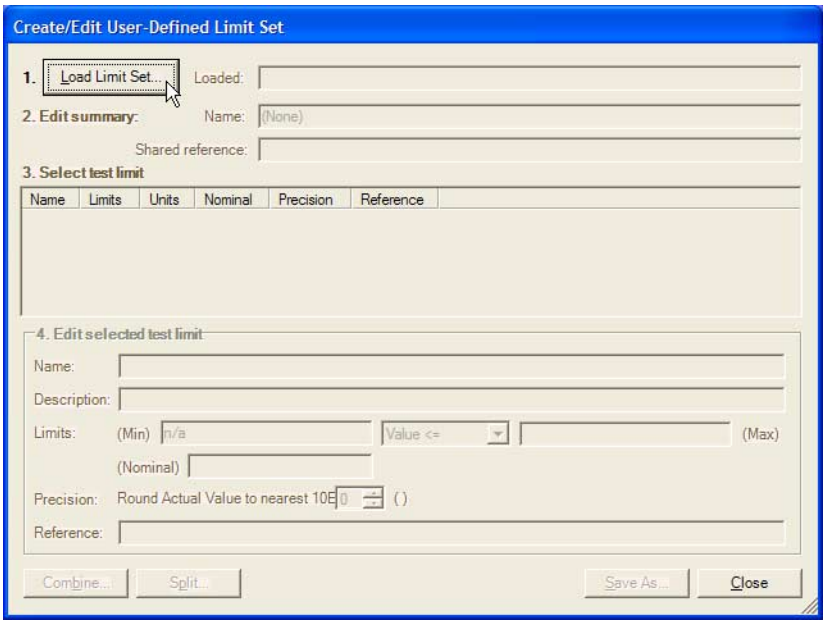
- DDR2 JEDEC Standard 79-2E, April 2008
- DDR3 JEDEC Standard 79-3C, November 2008

To create/edit limit sets

You can create new limit sets by modifying existing limit sets and saving them to new files.

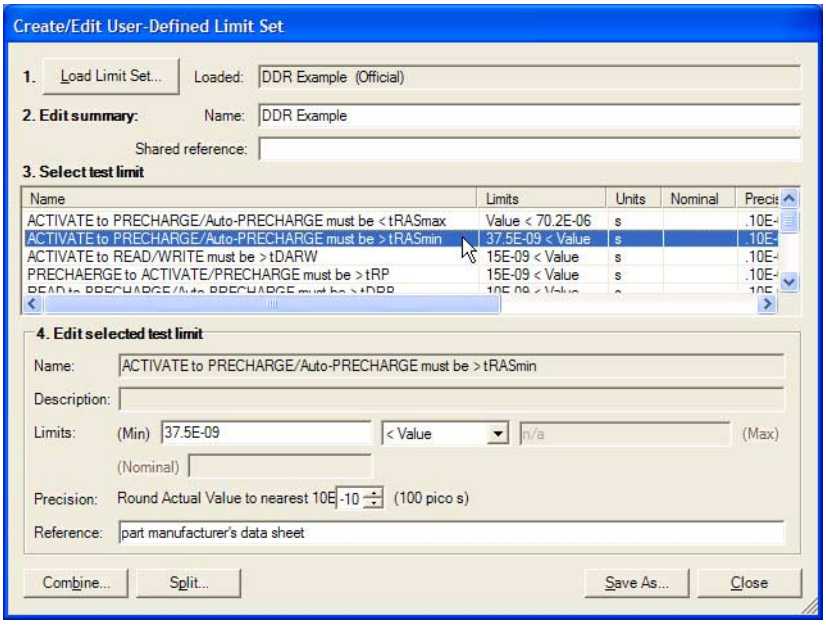
1 From the DDR validation tool's menu, choose **Tools>Compliance limits>Create/Edit limit set...**.

2 In the Create/Edit User-Defined Limit Set dialog, click **Load Limit Set...** to pre-load the dialog with the supplied example limit set (or a user-defined limit set).



3 Give the new limit set a unique name. If all of the tests come from the same reference, you can enter a base description (for example, document name) in the **Shared Reference** field and then add test-specific references (for example, page number) down below.

4 Select a limit to modify.



5 Modify the limit as desired. See also:

- "To split a combined limit" on page 23
- "To combine limits" on page 24

6 Repeat the last two steps until all limits requiring change are modified.

7 Click **Save As...** to save your custom limit set to a file. Enter the file name in the Save File As dialog.

Now, you can activate your newly-created limit set for use in the next run. See "To activate/refresh limit sets" on page 25.

When Loading Projects

When you load a project, the application will attempt to restore the limit set that was in use at the time the project was saved.

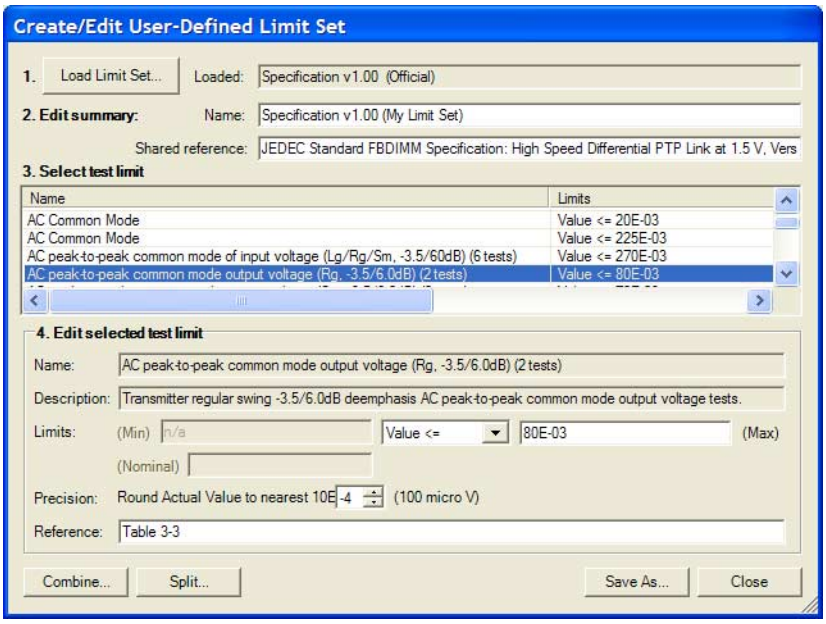
See Also

- "To set the test limits" on page 16 (for information on how to calculate the limits)

To split a combined limit

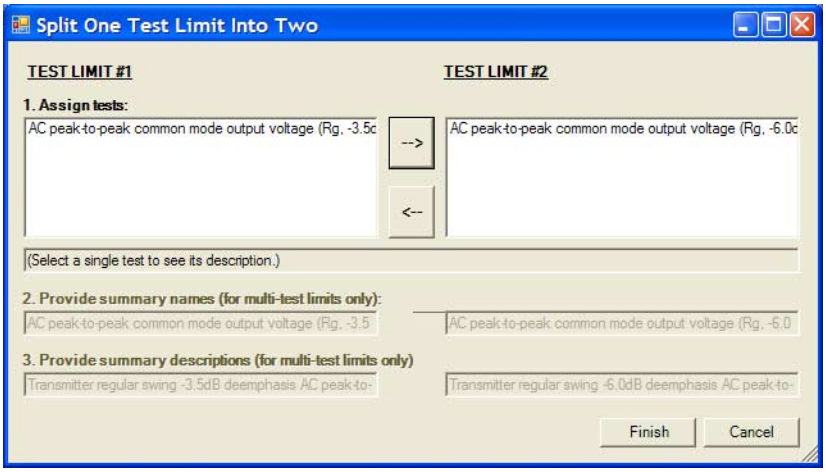
If a limit covers more than one test ID, you can split it into two limits.

1 In the Create/Edit User-Defined Limit Set dialog (see "To create/edit limit sets" on page 21), select the limit that covers multiple tests, and click **Split...**.



In this case, we are splitting a 2-test limit into two single-test limits.

2 In the Split Test Limit dialog, assign one of the tests to the new limit by selecting it and clicking the --> button.

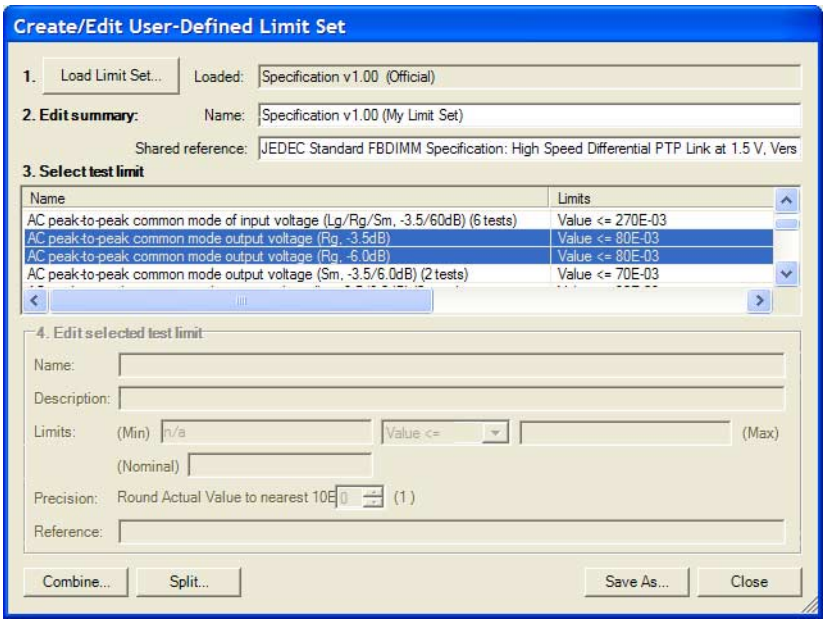


3 Click **Finish**.

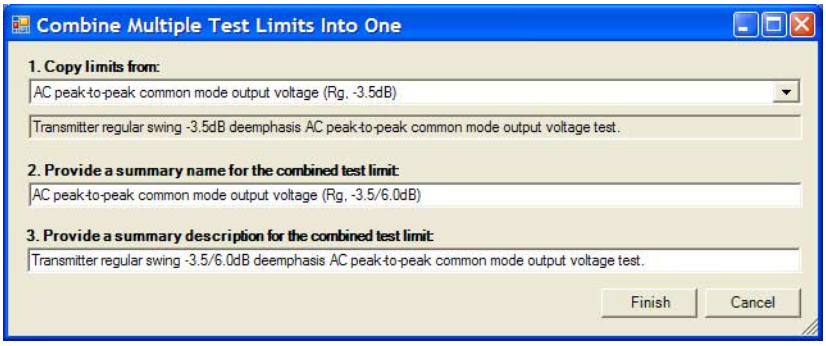
See Also • "To combine limits" on page 24

To combine limits

1 In the Create/Edit User-Defined Limit Set dialog (see "To create/edit limit sets" on page 21), select the limits you want to combine, and click **Combine...**.



2 In the Combine Multiple Test Limits dialog, select which limit to copy values from and provide summary names and descriptions.



3 Click **Finish**.

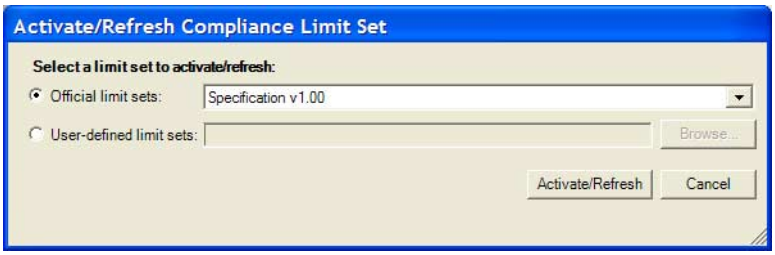
See Also • "To split a combined limit" on page 23

To activate/refresh limit sets

To load a previously defined limit set:

1 From the DDR validation tool's menu, choose **Tools>Compliance limits>Activate/Refresh limit set...**.

2 In the Activate/Refresh Compliance Limit Set dialog, select one of the official limit sets or a user-defined limit set.



3 Click **Activate/Refresh**.

NOTE If you have existing test results when you activate a different limit set, the application examines your results to see if any of them would experience a limit change when the different limit set is loaded. If any results would be affected in this way, the application tells you which ones they are and warns that they must be deleted.

See Also

- "To create/edit limit sets" on page 21

5 Setting Up the Test Environment

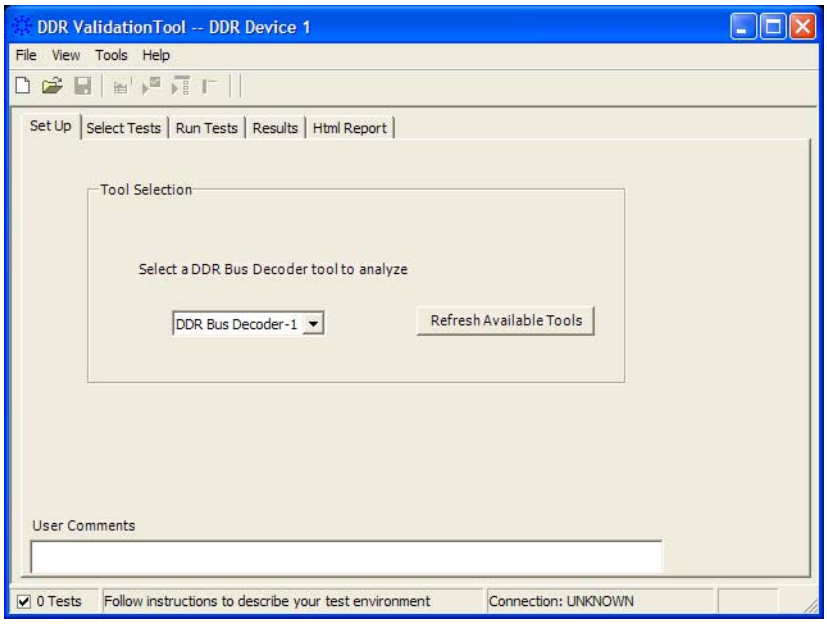
1 Click the Set Up tab.

2 If more than one DDR bus decoder exists in the logic analysis system setup, select which one to use for the compliance tests.

If only one decoder exists, it will be selected automatically.

If needed, select the **Refresh Available Tools** to update the list. You may need to refresh the list and select a new decoder if you load a new logic analyzer configuration file, or whenever you add or remove a decoder.

3 (optional) Describe the test for future reference. The **User Comments** will appear on the HTML report which is generated for the test.

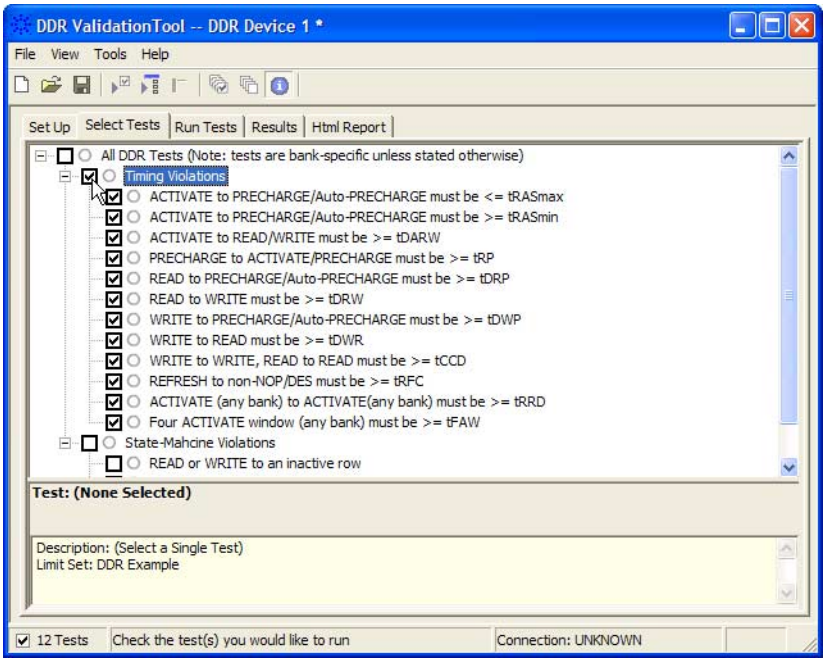


Next • "Selecting Tests" on page 29

6 Selecting Tests

1 Click the Select Tests tab.

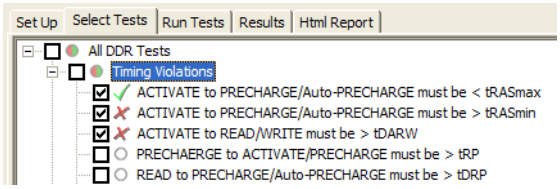
2 Check the tests you want to run.



Some things to note:

- Some tests might not make sense for your system. Do not select those tests.
- Checking a parent node/group will check all available sub-groups/tests.
- Unchecking a parent node/group will uncheck all sub-groups/tests.
- A parent node is checked if all subgroups are checked.
- A parent node is unchecked if ANY subgroup is unchecked.

When Tests Have Already Been Run



The marks have the following meanings:

✓	The test passed.
✗	The test failed.
○	The test has not been run, or no tests in the group have been run.
◌	The test is currently running.
◑	Some tests in the group have run and passed.
◑	Some tests in the group have run and failed.
◑	Some tests in the group have passed and some have failed; not all of the tests have been run.
●	Some tests in the group have passed and some have failed; all of the tests have run.
●	All tests in the group have run and passed.
●	All tests in the group have run and failed.

See Also

- "To set the test limits" on page 16 (for information on how to calculate the limits)
- (for an overview of the tests performed)

Next

- "Configuring Tests" on page 15

7 Running Tests

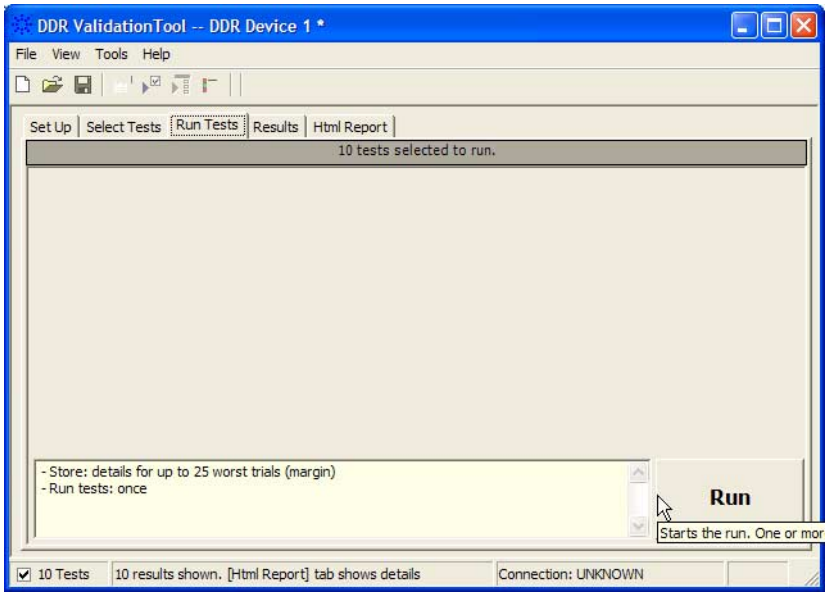
The Run Tests tab's settings let you run the selected tests once or multiple times. When you run tests multiple times, there are options for selecting which trials are stored and how long tests are run.

To run the selected tests once:

1 Start the test run.

There are several ways to run selected tests:

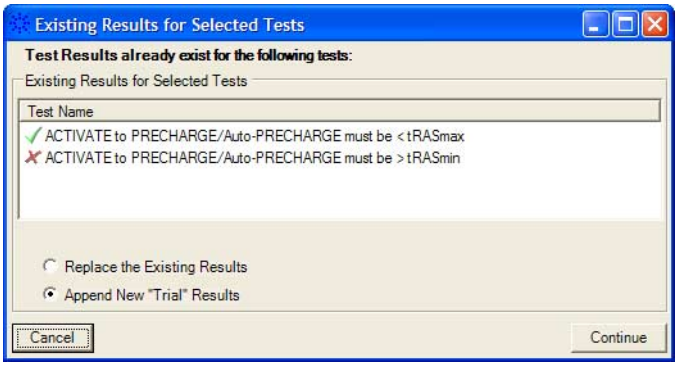
- Click  in the toolbar.
- Select a branch in the Select Tests tab; then, click  in the toolbar.
- Select the Run Tests tab, then click the big **Run** button.



2 If there are existing test results, you are asked if you would like to keep them or re-test (delete) them.

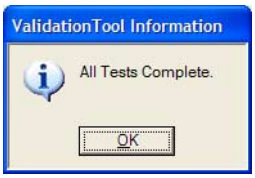
If you would like to keep the existing test results to compare against new results, select **Append New "Trial" Results**.

Select **Replace the Existing Results** if you would like to delete the existing test results.



3 While the tests are running, status dialogs appear to inform you about the test progress.

4 When the tests are complete, click **OK**.



See Also
- "To set the display preferences" on page 33

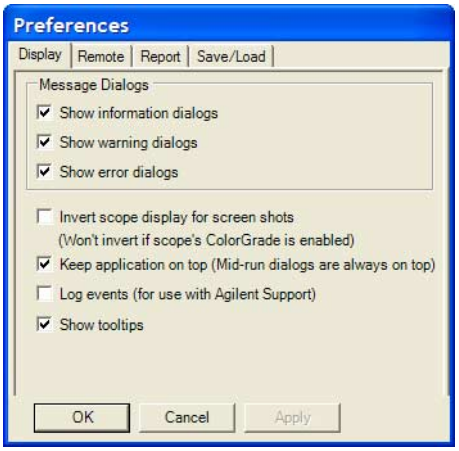
Next
- "Viewing Results" on page 35

To set the display preferences

Information, warning, and error conditions can occur while running tests. The display preferences let you choose whether message dialogs are shown. And, there are other display preferences that affect what happens as tests are run.

1 From the DDR validation tool's menu, choose **View>Preferences...**.

2 In the Preferences dialog, select the **Display** tab.



3 In the Display tab, you can choose to show the following types of message dialogs:

- Information dialogs.
- Warning dialogs.
- Error dialogs.

NOTE Messages that require you to make a choice, such as "OK/Cancel" and "Yes/No" are always enabled.

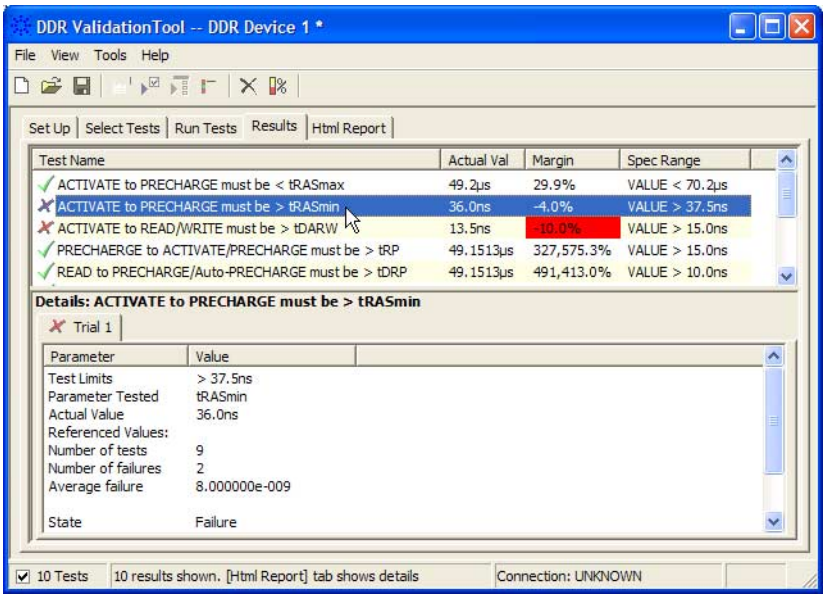
4 Also, you can choose to:

- **Invert scope display** – (Not used) Use a white background when the application captures the screen shots.
- **Keep application on top** – Always keep the application's main dialog on the top of the logic analyzer application. Note that the mid-run dialogs are always displayed on the top.
- **Log events** – Use this option only when directed to by Agilent Support (Note that this option degrades the runtime performance).
- **Show tooltips** – By enabling this option, the tooltips appear as you move the pointer over various controls in the application.

5 Click **Apply** to save the changes and click **OK** to close the Preferences dialog.

8 Viewing Results

1 Click in the toolbar, or click the **Results** tab.



The Results tab contains three resizable panes for test results information. If you select one of the tests in the top pane, details and reference images (if any) are shown in the lower panes.

TIP A quick way to reset all configuration options and delete all test results is to create a new project (see page 45). The new project will have default configuration options.

The tool will report a maximum of 1000 failures.

Each limit is measured as the time between two states. Each logic analyzer state has a number and a timestamp. In case of a failure, the numbers of the two states will be reported. Note that the time stamps are only as good as the time stamp resolution of the logic analyzer card being used (this resolution may be as coarse as 2ns; see the Specifications and Characteristics in the logic analyzer's online help for details).

If a test case is not encountered in the logic analyzer trace:

- In the details for the test, the number of tests will be 0.
- For limit tests, the "Actual Value" column will display "N/A."
- For pass/fail tests, the "Actual Value" column will display "Pass."

See Also
- "To change margin thresholds" on page 37

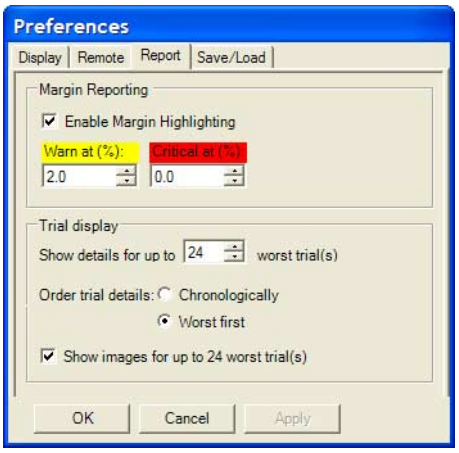
Next
- "Viewing/Exporting/Printing the Report" on page 39

To change margin thresholds

1 From the DDR validation tool's menu, choose **View>Preferences...**.

Or, when viewing the Results tab, click  in the toolbar.

2 In the Preferences dialog, select the **Report** tab.



3 In the **Margin Reporting** area, you can:

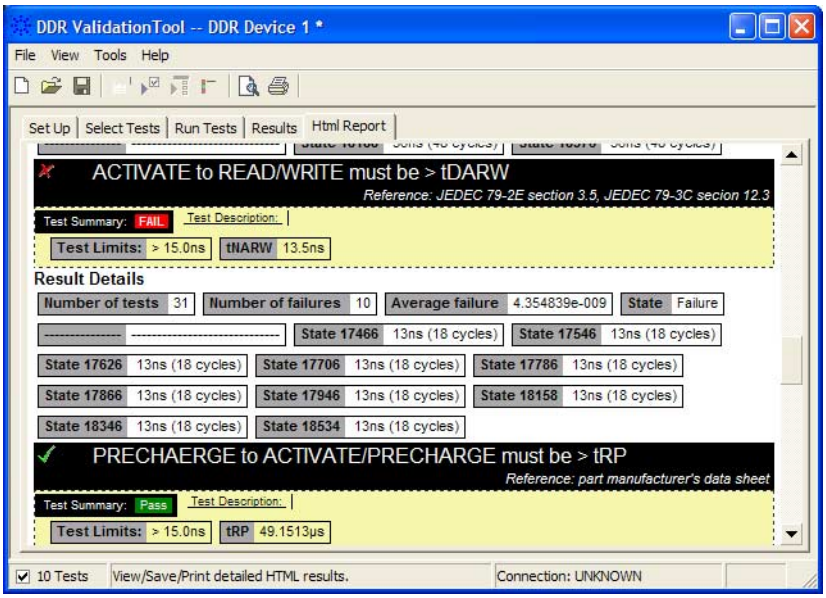
- Enable or disable margin highlighting.
- You can change the percent of margin at which to give warnings or critical failures.

4 Click **OK** to close the Preferences dialog.

NOTE The DDR validation tool runs the tests one time, so the Trial display options do not apply.

9 Viewing/Exporting/Printing the Report

- To view the HTML test report, click the **Html Report** tab.



See Also
- "To export the report" on page 40
- "To print the report" on page 42

Next
- "Saving Test Projects" on page 43

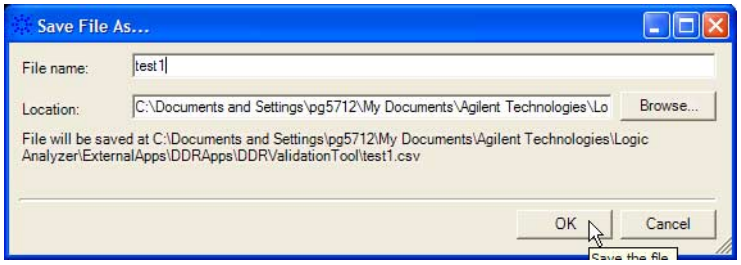
To export the report

1 From the DDR validation tool's menu, choose **File>Export Results>** from the menu.

There are two options for exporting the HTML test report: CSV or HTML.

To export results in CSV (comma-separated values) format

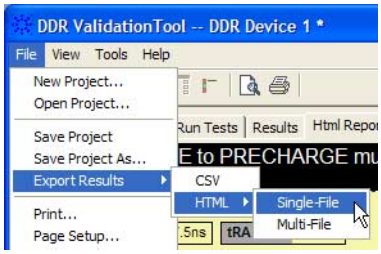
Select the CSV option to export the results as a comma-separated list of values.



The data format is shown in the first line of the exported *.csv file.

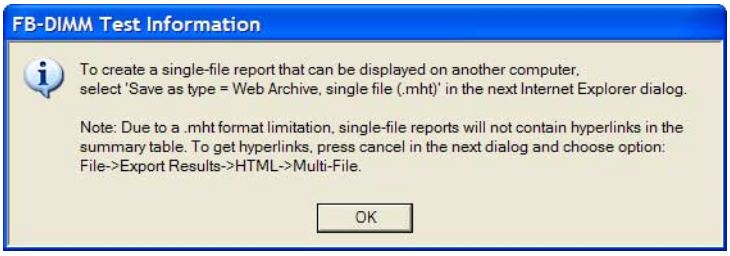
```
Test ID, Test Name, Measured Item, Trial 1 Value
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Number of t
ests ,"9"
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Number of f
ailures ,"0"
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Actual Valu
e,"4.92E-05"
100,"ACTIVATE to PRECHARGE/Auto-PRECHARGE must be < tRASmax",Margin,"29.
9"
```

To export the report in HTML format



There are two options for exporting HTML format test reports:

- **Single-File** — To save a single-file report, use the "save as" type "Web Archive, single file (.mht)".



NOTE Single-file reports will not contain hyperlinks in the summary table (due to a .mht format limitation). If you want these hyperlinks, use the multi-file format.

- **Multi-File** — If your report is large and you would like to use links within the report, select the **HTML>Multi-File** option. Selecting the multi-file option exports the results as a set of separate image and HTML files. It creates a folder with the specified name that may be copied to any computer.

  To view the exported report, open the HTML file stored in the folder.

To print the report

- To preview the HTML test report printout, click  or choose **File>Print Preview...** from the menu.
- To print the HTML test report, click  or choose **File>Print...** from the menu.

10 Saving Test Projects

To save test settings and results to the current project directory:

1 Choose **File>Save Project** from the menu.

To save test settings and results to a new project directory:

1 Choose **File>Save Project As...** from the menu.

2 In the Save Project As... dialog, enter the device name and location.

Project files will be saved in a directory whose name is the device name.

3 Click **OK**.

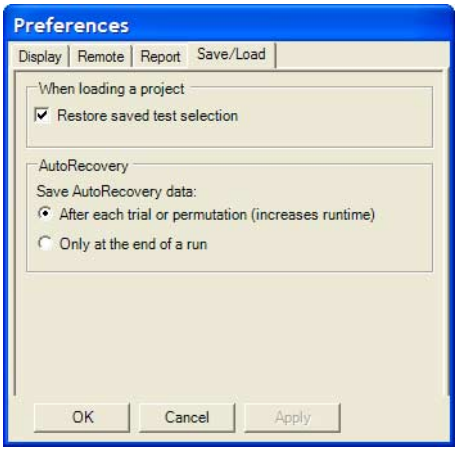
See Also

- "To set AutoRecovery preferences" on page 44

To set AutoRecovery preferences

1 From the DDR validation tool's menu, choose **View>Preferences...**.

2 In the Preferences dialog, select the **Save/Load** tab.



3 In the **AutoRecovery** area, you can choose:

- To auto-save results after each trial or permutation even if the entire multi-trial is not completed. This option enables full recovery.
- To auto-save results only upon the completion of the entire multi-trial.

4 Click **Apply** to save the changes and click **OK** to close the Preferences dialog.

11 Creating or Opening a Test Project

To create a new test project:

1 Choose **File>New Project...** from the menu.

A new, empty project, with all the default settings is created.

To open an existing test project:

1 Choose **File>Open Project...** from the menu.

2 In the Open dialog, browse to a test project directory and select the desired ".proj" file.

3 Click **Open**.

See Also

- "To set load preferences" on page 46

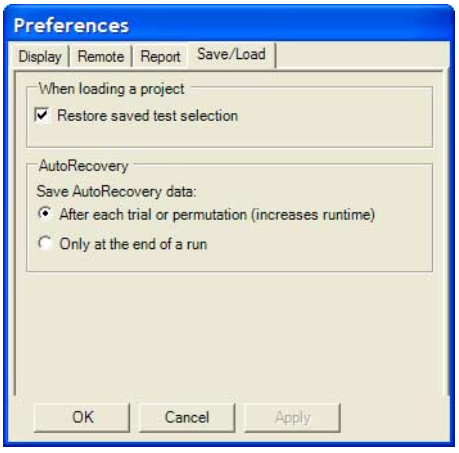
Next

- "Setting Up the Test Environment" on page 27

To set load preferences

1 From the DDR validation tool's menu, choose **View>Preferences...**.

2 In the Preferences dialog, select the **Save/Load** tab.



3 In the Save/Load tab, you can choose to restore saved test selections when loading a project.

4 Click **Apply** to save the changes and click **OK** to close the Preferences dialog.

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